Q.P. Code: 19EC0446 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Regular Examinations July-2021

ANALOG ELECTRONIC CICUITS

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Illustrate the basic concept of Feedback amplifier with suitable block diagram	L2	**6M**
	b	List the characteristics of negative feedback amplifiers.	L1	**6M**
		OR		
2	**a**	Compare and Contrast the various types of feedback amplifiers.	L2	**6M**
	b	An amplifier has open lop gain 1000 and feedback ration 0.04if the open lop gain changes by 10% due to temperature find the percentage change in gain of the amplifier feedback.	L4	**6M**

UNIT-II

3	**a**	Construct RC phase shift oscillator using BJT with necessary diagram and deriveits expression for frequency of oscillations.	L2	**6M**
	b	Determine the frequency of oscillations when a RC phase shift oscillator has R=100 kΩ, C=0.01μF and RC = 2.2 KΩ.	L5	**6M**
		OR		
4		Analyze an LC Oscillator with necessary equation.	L4	**12M**

UNIT-III

5	**a**	What are the four different configuration of differential amplifier?	L1	**6M**
	b	Compare and contrast ideal and practical op-amp.	L2	**6M**
		OR		
6	**a**	Explain dc characteristics of op-amp.	L2	**6M**
	b	Define the terms CMRR, common mode gain, differential mode gain, slew rate.	L1	**6M**

UNIT-IV

7	**a**	Design and explain the operation of inverting summing amplifier.	L3	**6M**
	b	The op-amp non-inverting summing circuit has the following parameters VCC =+15 V, VEE = -15V, R = R1= 1 kΩ, Rf = 2 kΩ, V1 = +2 V, V2 = -3 V, V3 =+4 V. Determine the output voltage V_o?	L5	**6M**
		OR		
8	**a**	Draw a neat circuit of astable multivibrator using op-amp and explainoperation with waveforms.	L2	**6M**
	b	Define duty cycle, if T_{on}=0.6 msec, Toff=0.4 msec. calculate percentage of dutycycle.	L5	**6M**

UNIT-V

9		Design a lowpass filter at a cut-of frequency of 15.9kHz with passband gain 1.5 and plot frequency response of this circuit.	L3	**12M**
		OR		
10	**a**	Draw and explain in detail about R-2R DAC	L2	**6M**
	b	The basic step of a 9 bit DAC is 10.3 mV. If "000000000" represents 0 V. What output isproduced if the input is"101101111"?	L5	**6M**

*** END ***